***PRACTICAL 2A: NAND GATE REPRESENTATION***

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3. This practical report (including circuit diagrams and code) is my own work.

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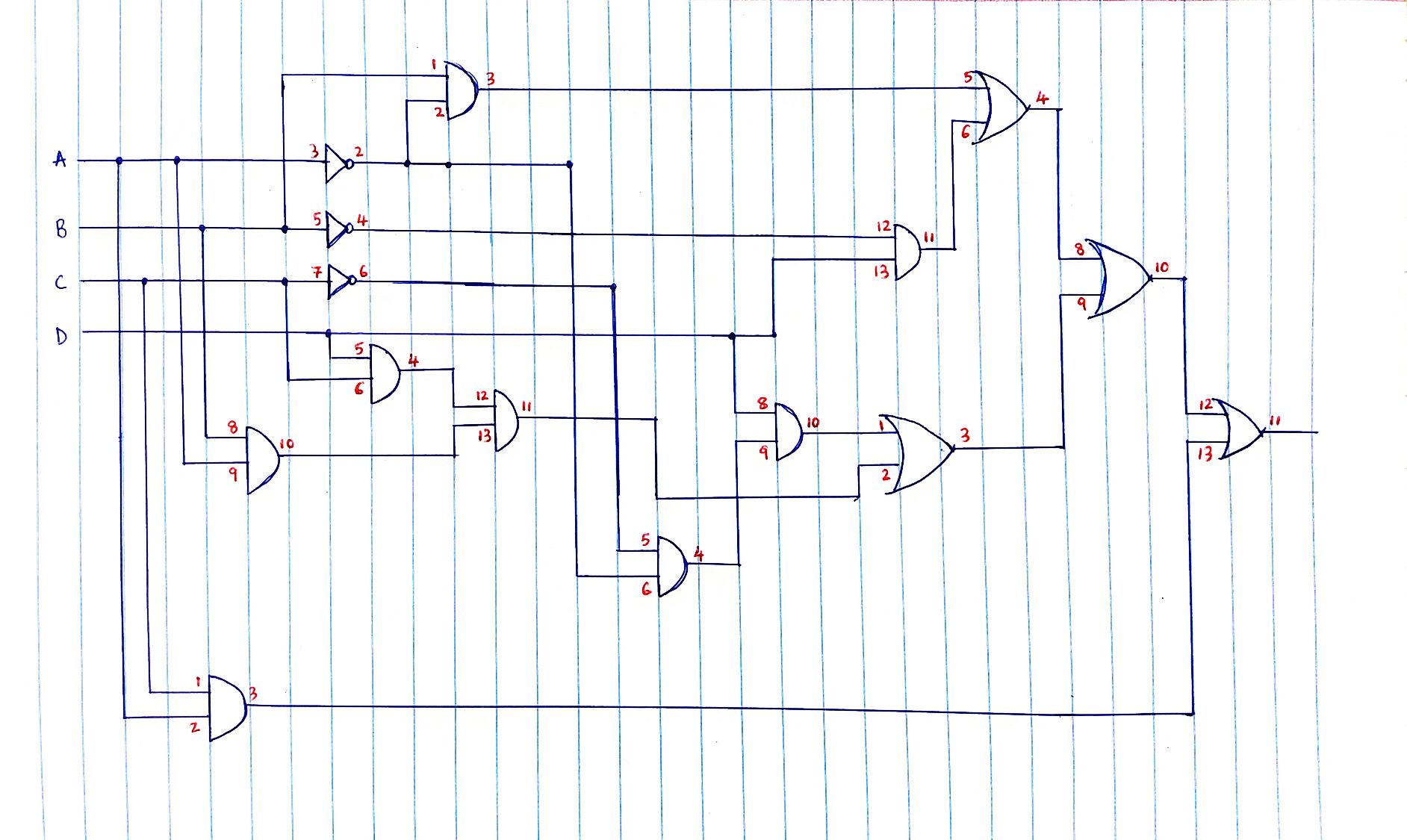
5. I acknowledge that copying someone else’s code, schematics or report, or part of it, is wrong, and declare that this is my own work.

18-04-2018

Signature Date

**Solutions**

a) Y = (A . B . C . D) + (Ā . B) + (A . C) + (!B . D) + (Ā . !C . D)



b) It will need Four 4000 series logic chips.

* 1 Quad 2-input OR-gate (4071)
* 2 Quad 2-input AND-gate (4081)
* 1 Hex Buffer Inverter (4049)

c)

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **(A.B.C.D)** | **(Ā.B)** | **(A.C)** | **(!B.D)** | **(Ā.!C.D)** | **Y** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |

d) **Sum of minterms = Sum of Products**

Y = (!A . !B . !C . D) **+** (!A . !B . C. D) **+** (!A . B . !C . !D) **+** (!A . B . !C . D) **+** (!A . B . C . !D) **+** (!A . B . C . D) **+**

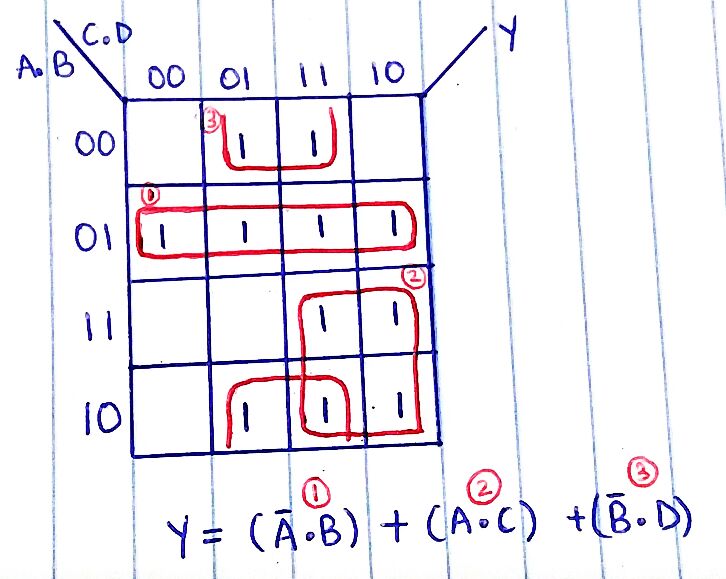
(A . !B . !C . D) **+** (A . !B . C . !D) **+** (A . !B . C . D) **+** (A . B . C . !D) **+** (A . B . C . D)

e) **Product of maxterms = Product of Sum**

Y = (A + B + C + D) **.** (A + B + !C + D) **.** (!A + B + C +D) **.** (!A + !B + C + D) **.** (!A + !B + C + !D)

f)

**KARNAUGH MAP**



g) **Y = (!A . B) + (A . C) + (!B . D)**

Y = !( !((!A . B) + (A . C) + (!B . D)) )

Y = !( !((!A . B)) . !((A . C)) . !((!B . D)) )

Y = !( !(!(A.A) . B) . !(A . C) . !(!(B.B) . D) ) //Simplified Version

For more complex but detailed circuit; join two of the expressions with a NAND gate and then NAND

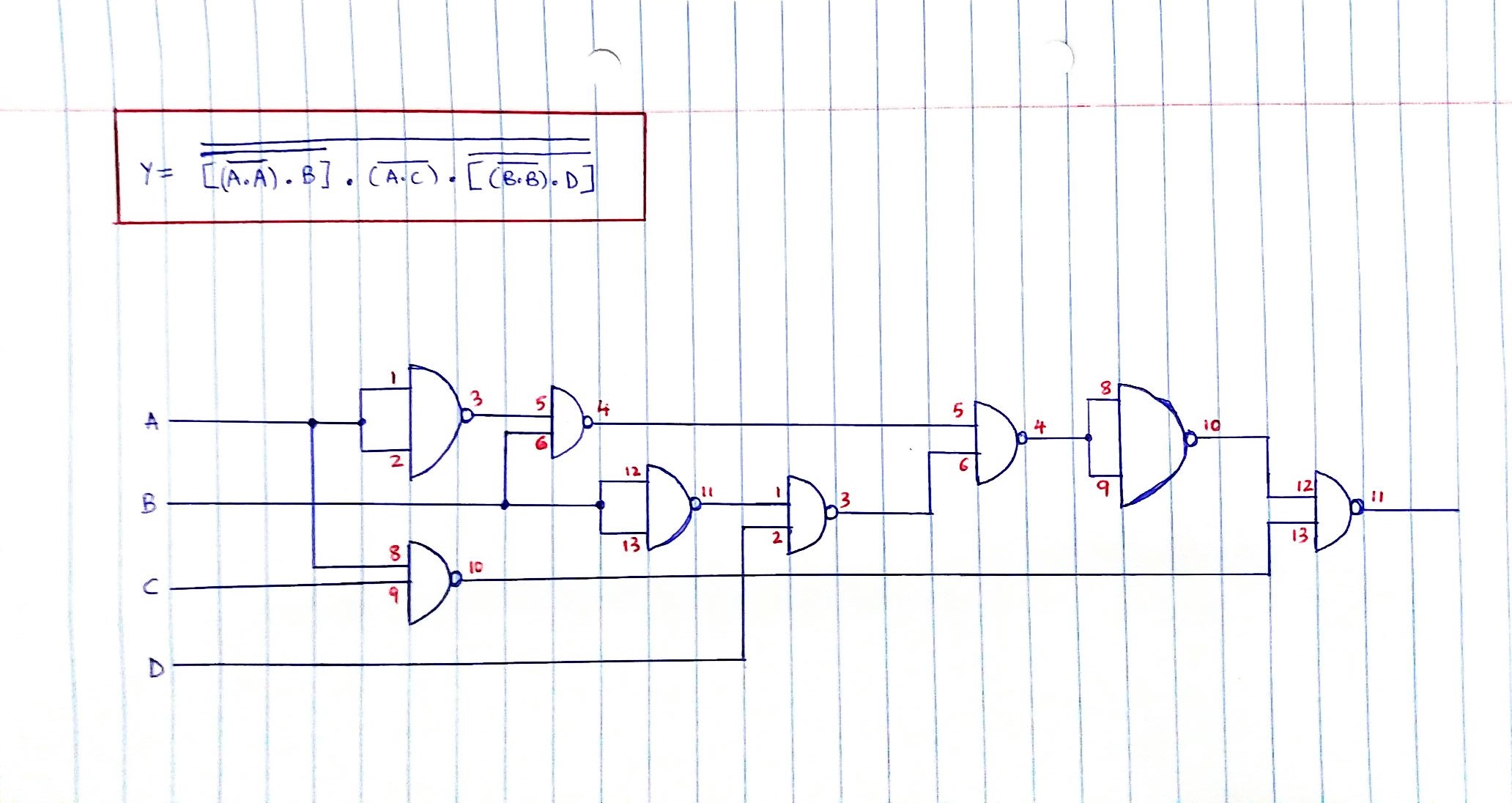
the output with itself

Y = !( !(!(A.A) . B) . !(!(B.B) . D) . !(A . C) )

Y = !( !( !(!(A.A).B) . !(!(B.B).D) ) . !(A . C) )

Y = !( !( !( !(!(A.A).B) . !(!(B.B).D) ) . !( !(!(A.A).B) . !(!(B.B).D) ) ) . !(A . C) )

h)



j)

Y = !( !(!(A.A) . B) . !(A . C) . !(!(B.B) . D) )

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **!(A.A)** | **!( !(A.A) .B)** | **!(A.C)** | **!(B.B)** | **!( !(B.B) .D)** | **Y** | **VERIFIED** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |